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Title:

METHOD AND APPARATUS USING SWITCHES FOR POINT TO POINT BUS OPERATION

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METHOD AND APPARATUS USING FET SWITCHES FOR POINT TO POINT BUS OPERATION

This application is a continuation-in-part (CIP) of application Ser. No. 09/741,821 (Attorney docket M4065.0406/P406), filed on December 22, 2000, which is hereby incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to improving the signal integrity and performance of a high speed bus for data communications.

BACKGROUND OF THE INVENTION

Memory device manufacturers are under continuous pressure to increase the performance and reduce the cost of memory devices. Memory systems for computers typically provide many memory devices on a common multidrop bus to allow larger storage and transmission capacities than can be obtained with a single memory device. To improve the maximum throughput of the bus, data communicated to and from the memory devices may be multiplexed for transmission on the bus, thereby reducing the pin count of a memory bus master or controller. For example, a 64-bit wide data word may be transmitted over a 16 bit data bus as four successive 16-bit data word portions.

In addition, such systems typically include user upgradable or replaceable components to allow future expansion or repair of the memory subsystems. Typically, these systems are upgraded on a module basis, where the memory module (e.g., a dual in-line memory module or DIMM) includes several memory devices on a small printed circuit board (PCB), and the module plugs

into a connector that provides an electrical connection to the memory subsystem bus.

Connection of multiple memory devices to the bus can degrade the performance of the bus since the modules are typically connected in a configuration having electrical stubs which cause signal reflections on the bus. These reflections degrade signal integrity, thus limiting the maximum speed and bandwidth of the system. A robust electrical design is required in a high speed multidrop memory bus since the signal integrity must be acceptable throughout the system for lightly loaded systems, that is, where only a small number of module slots are populated, as well as heavily loaded systems where every module slot, or nearly every module slot, is populated.

In addition, although high speed communication between memory devices can be done using a transmission line or bus that is properly terminated, the speed at which data is passed can be limited by the capacitance of the memory devices and the resistance of circuit elements used to terminate the bus. As noted, bus reflections can limit the speed of data transmission as well.

Accordingly, there is a strong desire and need to improve the performance characteristics of memory bus systems and other data bus systems in order to permit high speed operation with minimal degradation of signal integrity due to bus reflections.

SUMMARY OF THE INVENTION

The present invention provides a method and associated apparatus for improving the performance of a high speed data bus, e.g., a memory bus. The invention mitigates bus reflections caused by electrical stubs by connecting

contemporaneously-selected system components in a stubless or substantially stubless configuration using switches, for example field effect transistor (FET) or other electronic switches.

In one aspect, the invention provides a high speed segmented bus in which the individual bus segments are connected by switches. The switches are configured to connect those segments required for communications between currently selected data input/output devices, e.g. memory modules, and disconnect the remaining segments. The resulting bus connects the currently selected data input/output devices in an essentially point-to-point communications configuration for reduced signal reflections and improved signal integrity.

In another aspect, the invention provides a method of data communication between data exchanging devices which maintains a substantially stubless environment. A first set of I/O pins and a second set of I/O pins are provided at data input/output devices, e.g., memory modules, for connecting respective first and second segments of a data bus through a switching circuit, e.g., a FET switch, at each data input/output device on the bus. Data is received and transmitted on the data bus using at least the first set of I/O pins, and data on the data bus is selectively passed through from the first bus segment to the second bus segment and from the second bus segment to the first bus segment using the switching circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other features, advantages and structural implementations of the invention will become more apparent from the detailed

description of the exemplary embodiments of the invention given below with reference to the accompanying drawings in which:

FIG. 1 illustrates a bus topology formed in accordance with a first exemplary embodiment of the invention;

FIG. 2 illustrates in greater detail a portion of FIG. 1;

FIG. 3 illustrates a modified first embodiment of the portion shown in FIG. 2;

FIG. 4 illustrates a memory module formed in accordance with a first exemplary embodiment of the invention;

FIG. 5 illustrates a bus topology formed in accordance with another exemplary embodiment of the invention;

FIG. 6 illustrates a bus topology formed in accordance with another exemplary embodiment of the invention;

FIG. 7 illustrates a timing example in accordance with an exemplary embodiment of the invention;

FIG. 8 illustrates a bus topology formed in accordance with another exemplary embodiment of the invention;

FIG. 9 illustrates a portion of the topology of FIG. 1 in accordance with another exemplary embodiment of the invention;

FIG. 10 illustrates a processor system formed in accordance with another exemplary embodiment of the invention;

FIG. 11 illustrates a bus topology formed in accordance with another exemplary embodiment of the invention;

FIG. 12 illustrates a bus and switch topology formed in accordance with another exemplary embodiment of the invention;

FIG. 13 illustrates a bus and switch topology formed in accordance with another exemplary embodiment of the invention;

FIG. 14 illustrates a bus and switch topology formed in accordance with another exemplary embodiment of the invention;

FIG. 15 illustrates a bus and switch topology formed in accordance with another exemplary embodiment of the invention;

FIG. 16 illustrates a bus and switch topology formed in accordance with another exemplary embodiment of the invention;

FIG. 17 illustrates a bus and switch topology formed in accordance with another exemplary embodiment of the invention; and

FIG. 18 illustrates a bus and switch topology formed in accordance with another exemplary embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention provides a bus system including switches which can be used to interconnect data input/output devices and/or bus segments. While the invention is described below with reference to a bus system for a memory system, including memory modules as representative data input/output devices, it should be understood that the bus and switch topology of the invention may be used with any type of data input/output device. Likewise, it should be understood that the memory controller described in the context of a memory system may be a bus controller for use with other data input/output devices besides memory modules.

Referring to FIG. 1, an exemplary processor system 20 including a memory subsystem is illustrated employing a high speed bus system. The processor system 20 includes several data input/output devices, which take the form of memory modules 24, 26, connected to a memory controller 31 with a segmented data bus 28, and a processor 22 connected to the memory controller

31 via a conventional bus 29. Each of the memory modules 24, 26, as well as the memory controller 31, has an associated integrated interface circuit 30 connecting each to the segmented data bus 28. Each integrated interface circuit 30 permits data exchange between the segmented data bus 28 and another data pathway, for example, a second data bus 32, shown at each of the respective memory modules 24, 26. The second data bus 32 is connected to individual memory devices, e.g., DRAM chips, provided on the modules 24, 26.

The segmented data bus 28 may be a multidrop bus and may be terminated by a bus terminator, for example a bus terminating resistor 38. The bus terminating resistors may be located at the memory controller as shown in FIG. 1, at one end of the bus as shown in FIG. 8, at the interface circuit 30 as shown in FIGS. 2, 3 and 13, at the memory modules 24, 26 as shown in FIG. 12, and/or at each memory device 54, 56, 60 as shown in FIG. 14. The bus terminating resistor 38 may be a switched terminator to permit switchable termination (i.e., termination enabled (ON) or termination disabled (OFF)) for varying data transfer operations. For example, the switched terminator 38 at the memory controller 31 (FIG. 1) may be enabled during data READ operations, but may disabled during data WRITE operations. Similarly, the switched terminator 38 at the memory device 54, 56, 60 (FIG. 14) selected for data operations may be enabled during data WRITE operations, but may be disabled during data READ operations. The switched terminator 38 may provide source termination for alleviation of the effect of bus reflections, improving data transfer performance.

Although two memory modules 24, 26 are illustrated, it should be understood that any number of memory modules may be connected to bus 28 in accordance with the invention.

The segmented data bus 28 may be a conventional m-bit parallel bus having command and address paths, data paths, and clock (timing) paths. The segmented data bus 28 may have a bus width of any number of parallel data paths, but typically has fewer data paths than a second data bus 32 attached to the interface circuit 30. As one example, the segmented data bus 28 may be 16 bits wide (16 data paths) while the second data bus 32 may be 64 bits wide (64 data paths). Accordingly, and as described below, data from the memory devices connected to the wide bus 32 can be multiplexed by interface circuit 30 onto the narrower bus 28, while data on bus 28 can be demultiplexed and placed on bus 32. Accordingly, bus 28 operates at a higher data transfer speed than bus 32, enabling memory modules 24, 26 to use lower speed memory devices than would otherwise be required with a high speed bus.

Since the segmented data bus 28 has a smaller number of data paths than data bus 32, the integrated interface circuits 30 connect to the segmented data bus 28 with a low pin count connection.

Each interface circuit 30 includes a switching circuit, e.g., a FET switch 39 as illustrated in FIGS. 2 and 3, through which the segmented data bus 28 is connected for communication with the memory modules 24, 26. In this way, memory modules 24, 26 on the segmented data bus 28 can be connected in a "daisy chain." This configuration substantially eliminates bus reflections caused by electrical stubs by selectively connecting system components in a substantially stubless configuration which improves the data rate which can be achieved on bus 28.

For example, when a memory module 26 is selected for operations, e.g. a READ or WRITE operation, a switching circuit, e.g., FET switch 39, at the memory module 26 disconnects the remainder of the segmented data bus 28 including segment 28c. Simultaneously, a switching circuit, e.g., FET switch 39,

at the memory module 24 permits data to pass through between bus segment 28a and bus segment 28b. In this way, the memory module 26 and the memory controller 31 may be connected in a point-to-point data connection substantially free of stubs during the READ or WRITE operation.

Although the switching circuits, e.g., FET switches 39, are described as being located on the memory modules 24, 26, they may alternatively be positioned at other locations, for example, on a memory device 54, 56, 58, 60, or at locations external to both the memory modules 24, 26 and memory devices 54, 56, 58, 60. For example, FIGS. 2 and 3 illustrate embodiments of the invention in which the switch, e.g., FET switch 39, is located on the interface 30, which is located on the memory module 24. In another example, as shown in FIG. 14, one or more switches 302''' may be located on respective memory devices 54, 56, 58, 60. In another example, as shown in FIGS. 12 and 16, each switch (302' in FIG. 12 and 39 in FIG. 16) may be located external to both the memory modules 24, 26 and the memory devices 54, 56, 60.

For embodiments of the invention including external switches, as shown in FIGS. 12 and 16, the switches (302', FIG. 12; 39, FIG. 16) may advantageously employ differing semiconductor technology from the memory devices or other integrated circuit structures. For example, each of the external switches 302', 39 may be formed using Gallium Arsenide (GaAs) semiconductor technology for increased switching performance.

Referring back to FIG. 2, which shows the switch 39 provided on the module 24, each integrated interface circuit 30 may be connected to the segmented data bus 28 by first 42 and second 44 sets of I/O pins (pads). A first set of I/O pins 42 may be connected to a first bus segment 28a and a second set of I/O pins 44 may be connected to a second bus segment 28b. The first and second sets of I/O pins 42, 44 are connected internally within the integrated

interface circuit 30 through the switching circuit, which as noted is illustrated in FIG. 2 as FET switch 39. The I/O pins 42 are also connected to a conversion circuit 45 which converts data appearing on the segmented data bus 28 for use on a second bus 32. For the example earlier described of a 16 bit data path on bus 28 and a 64 bit data path on bus 32, each set of I/O pins 42 will contain 16 pins for the data path, as shown in FIG. 9. Likewise, there would be 16 I/O pins 44 for connection with downstream bus segments, e.g., 28b.

The FET switch 39 in FIG. 2 optionally connects the first bus segment 28a with the second bus segment 28b for optional pass-through of data on the segmented data bus 28. It should be remembered that FIGS. 2, 3 only show one bus data path and that therefore only one FET switch 39 is shown, but in actuality each data path (16 in the example given) will have respective bus segments 28a, 28b and an associated FET switch 39.

Data on the segmented data bus 28 may pass through the I/O pins 42, 44 and FET switch 39 and pass to and from downstream memory modules, or may be optionally received by the interface circuit 30 in which case the FET switch 39 on an associated module will be open. Any data received at an interface circuit 30 may then be converted in conversion circuit 45 for use on the second bus 32. Likewise, data on bus 32 may be converted by conversion circuit 45 and passed through pins 42 back to the memory controller 31. Thus, during typical operations, the FET switch 39 is configured to disconnect the first bus segment 28a from the second bus segment 28b while the interface circuit 30 is receiving transmitted data through circuit 45 between bus segment 28a and the second bus 32. Likewise, the FET switch 39 is typically configured to connect the first and second bus segments 28a, 28b and pass data through while the interface circuit 30 is not selected for operations.

Data may be selectively received by the interface circuit 30 according to a selection signal received at the integrated interface circuit 30. The selection signal may be available to the interface circuit 30 on a conventional non-segmented memory system command and address bus 135, as shown in FIG. 2. For example, signals received from a conventional command and address bus 135 are captured and decoded by circuitry 133 and may contain instructions for controlling reception of data at integrated interface circuit 30, for example, a WRITE command directing the integrated interface circuit 30 to receive data available on the segmented data bus 28 for storage at a memory device connected to the second data bus 32. The command and address bus 135 may also provide each memory module 24, 26 with address signals for read and write operations.

Signals from the capture/decode circuitry 133 may be passed on to the multiplexer/demultiplexer 46 and/or the switching circuit 39 when the interface circuit 30 is selected for operations, e.g., a WRITE command, to activate the conversion circuit 45 and disconnect the first and second bus segments 28a, 28b. Thus, point-to-point data communications may then be performed between the interface circuit 30 and another system device, e.g. a memory controller 31 (FIG. 1).

As an alternative to the configuration shown in FIG. 2, selection signals may be made available to the interface circuit 30 on a segmented command and address bus 235, as illustrated in FIG. 11, having a construction similar to the segmented data bus 28 for selectively passing selection signals and other information used by the interface circuit 30 through closed switches to downstream command/address bus segments, or prevents such passage by an open switch. Referring to FIG. 11, the segmented command and address bus 235 may include segments 235a, 235b, 235c, connecting the integrated interface circuits 30 of the system components.

An alternative to the use of selection signals such as those provided on the command and address bus 135 is to embed selection signals in signals transmitted on the segmented data bus 28 shown in FIG. 1 during times when no data is being transmitted.

Referring again to FIG. 2, the second data bus 32 may have operating requirements that differ from those of segmented data bus 28, for example the second data bus 32 may be a higher pin count, higher voltage, lower data rate bus that uses a data encoding different from that of the segmented data bus 28. Therefore, the conversion circuit 45 may convert the data received from the segmented data bus 28 for use on the second data bus 32. The conversion circuit 45 may include a multiplexer/demultiplexer 46 for converting the data rate and number of data paths (e.g., between 16 and 64 data paths), a coder/decoder 47 for appropriately coding/decoding the data between buses 28 and 32, and a voltage converter 48, which permit data available on the segmented data bus 28 to be appropriately configured for the second bus 32 and vice versa.

As shown in FIG. 2, voltage conversion may be performed using a voltage converter 48 provided between the segmented data bus 28 and the multiplexer/demultiplexer 46. This is not required, however, and as illustrated in the integrated interface circuit 30' shown in FIG. 3, voltage conversion may instead be performed at a voltage converter 48 located between the second data bus 32 and the multiplexer/demultiplexer 46. Of course, if voltage conversion is not needed, voltage converter 48 may be omitted.

The conversion circuit 45 may convert data on the segmented data bus 28 for use on the second data bus 32, but the corresponding conversion in the opposite direction (i.e., from the second data bus 32 to the segmented data bus 28) may also be performed by the conversion circuit 45 in accordance with the invention.

The integrated interface circuit 30 may be turned off when the second data bus 32 is not active, for example in response to selection signals received on the command and address bus 135. When selection signals received indicate that the interface circuit 30 is turned off, the switching circuit 39 connects the first and second segments 28a, 28b of the segmented data bus 28. When selection signals indicate that the interface circuit 30 is turned on, the switching circuit 39 disconnects the first segment 28a from the second segment 28b to form a point-to-point communications path for data being communicated using the interface circuit 30.

The switching circuit 39 may comprise, for example, a field effect transistor (FET) switch, for example a p-channel transistor as illustrated in FIGS. 2 and 3. The p-channel transistor defaults to the on, or pass-through, state in which data is permitted to pass between bus segments 28a, 28b, 28c. When the gate of the p-channel transistor is activated, the bus segments on either side of the switch are disconnected and data is not permitted to pass through. In this way, a selection signal received at the capture/decode circuitry 133 simultaneously activates the conversion circuit 45 and disconnects the first and second bus segments 28a, 28b, so that the interface circuit 30 and another system component may communicate in a substantially stubless environment using an essentially point-to-point communications path. It should be understood that other types of known switching circuits 39 may also be used in place of the FET switch.

As noted, one potential use of segmented bus 28 is for a memory system including memory modules 24, 26. FIG. 4 illustrates one of the memory modules 24, which includes a plurality of memory devices 54, 56, 58, 60, mounted on a printed circuit board with the integrated interface circuit 30. Each of the memory devices 54, 56, 58, 60 is connected to a memory bus 32 that also connects to the integrated interface circuit 30. The integrated interface circuit 30

includes a switching circuit, for example a FET switch 39 (FIG. 2), connected between bus segments. In addition, the integrated interface circuit 30 connects to the segmented data bus 28 using the first and second sets of I/O pins 42, 44.

In operation, the integrated interface circuit 30 receives/transmits data from/to another device connected to the segmented data bus 28, e.g., from a memory controller 31, and converts the data to/from the memory bus 32 which is coupled to the individual memory devices 54, 56, 58, 60. Any necessary data rate, voltage, or other conversions which may be required for data to be exchanged between the segmented data bus 28 and the memory bus 32, for example between the memory controller 31 and the memory devices 54, 56, 58, 60, are performed at interface 30. For example, referring to FIGS. 1 and 4, the integrated interface circuit 30 may be connected to the memory controller 31 via the segmented data bus 28, which operates at a 1 Gbit/sec data rate, 1 volt voltage level, and a narrow bus width (low pin count) of 16 data paths (bits). In contrast, the memory bus 32, connected to the integrated interface circuit 30, may operate at a 250 Mbit/sec data rate, 1.8 volt voltage level, and a wide bus width (high pin count) of 64 data paths (bits). For a memory WRITE operation initiated by the processor 22 or the memory controller 31 to store data using the memory devices 54, 56, 58, 60, the WRITE data is transmitted on the segmented data bus 28 from the memory controller 31 to the integrated interface circuit 30, the WRITE data is converted, and transmitted on the memory bus 32 to one or more of the memory devices 54, 56, 58, 60. READ data from the memory devices 54, 56, 58, 60 flows in the opposite direction to the memory controller 31.

FIG. 7 illustrates a timing example for data exchange between a 16-bit segmented data bus 28 and a 64-bit memory bus 32. The integrated interface circuit 30 may receive 16 bits of data at time t=1, t=2, t=3, and t=4. At time t=4, after the integrated interface circuit 30 has received a total of 64 bits of data, from

the segmented data bus 28, the received data may be passed to the memory bus 32 via the 64 data paths of the memory bus 32. This data rate conversion and/or buffering may be performed using the multiplexer/demultiplexer 46 (FIG. 2). Any other voltage conversions or data encoding/decoding functions needed are performed at the interface circuit 30 as described above and illustrated in FIGS. 2 and 3.

For a memory READ operation, the converse data transfer operation from the memory devices 54, 56, 58, 60, to the memory controller 31 is performed. That is, 64 bits of data on bus 32 are multiplexed by interface circuit 30 as four 16 bit data segments which are sequentially placed on segmented data bus 28.

FIGS. 4-5 also illustrate that the memory devices 54, 56, 58, 60, attached to the memory bus 32 may be mounted on a single memory module 24 (FIG. 4) or, alternatively, may be mounted on respective printed circuit boards (PCBs) or other support structure (FIG. 5), but nevertheless each memory device 54, 56, 58, 60 is connected to the memory bus 32.

The memory controller 31 is connected to the segmented data bus 28 and may exchange data with each of the integrated interface circuits 30. Alternatively, as shown in FIG. 6, the memory controller 31 may be omitted and the processor 22 may be connected to the segmented data bus 28. In this arrangement, the processor 22 may exchange data over the segmented data bus 28 with each of the integrated interface circuits 30, which in turn communicate with memory devices on the memory modules 24, 26 over the second data buses 32.

The embodiment illustrated in FIG. 6 advantageously eliminates the need for a separate memory controller chip conventionally used as an intermediary between the processor and the memory devices in a typical computer system. For an exemplary system in which the integrated interface circuit 30 adds latency to

data communications between devices connected to the segmented data bus 28 and the second data bus 32 (FIG. 1), any loss in performance may be alleviated by elimination of a conventional memory controller. Some functions formerly provided by a conventional memory controller, such as memory address-to-module mapping, may be performed instead at the processor 22. Other functions formerly performed by a conventional memory controller, such as voltage conversion, may be performed by the integrated interface circuit 30. Thus, the latency associated with the memory controller may be mitigated while still permitting processors and memory devices of differing voltage levels to interoperate.

Latency could also be improved by including an additional multiplexer in the integrated interface circuit 30 for performing multiplexing tasks ordinarily performed at individual memory devices on the second data bus 32. This would allow the multiplexing tasks to be performed at the higher operating rate of the integrated interface circuit 30.

Thus far all exemplary embodiments of the invention have been described as using one switch circuit to pass data either to a selected memory module, e.g., 24, or to a downstream bus segment, e.g., 28b. However, two switch circuits may also be used as shown in FIG. 17. FIG. 17 shows an exemplary embodiment of the invention including a first switch 39 and a second switch 439 associated with each input/output device, e.g., each memory module 24, 26. The first switch 39 can be configured to selectively connect memory modules 24, 26 to the memory controller 31 via the control circuits 442. For example, the first switch 39 may selectively disconnect the memory controller 31 from the other memory module 26. Simultaneously, the second switch 439 can be configured to selectively connect the first memory module 24 to the memory controller 31 via the control circuits 442. Preferably, the first switch 39 does not

pass data while the second switch 439 passes data between the first memory module 24 and the memory controller 31, so as to provide a point-to-point data connection for improved communication performance between the first memory module 24 and the memory controller 31. Likewise, preferably the first switch 39 passes data while the second switch 439 does not pass data, so as to permit improved communications between the memory controller 31 and the other memory module 26 by reducing bus reflections, resistance, and/or capacitance that could degrade performance. Each of the switches 39, 439 corresponding to the other memory modules 26 may be controlled by the control circuits 442 in a similar fashion.

In another example, a simple two-way switch may be used in lieu of the switching circuit 39 shown in FIGS. 2 and 3. FIGS. 12-15 show several exemplary embodiments of the present invention using simple two-way switches 302' to connect the memory controller 31 and a selected memory module 24 (FIGS. 12, 13) or individual memory devices 54, 56, 58, 60 (FIGS. 13, 14) in a substantially stubless configuration.

FIG. 12 shows a bus and switch topology in which each of the two-way switches 302" is located separately from other system elements, for example two way switches 302" may be located on a motherboard 310. The two-way switches 302" may be controlled by a selection signal transmitted, for example, on the command and address path 135. In this case, a decoder 315 is required to decode a command for a particular switch. Alternatively, the selection signal may be included in data transmitted on the data bus 28 or a separate selection signal path for each switch 302" may be provided on the motherboard 310. When the selection signal selects a certain memory module 24, 26 for operations, the two-way switches 302" can be simultaneously configured to connect the module (e.g., 24) containing the memory devices (e.g., 54, 56, 58, 60) with the memory

controller 31. For example, if the first memory module 24 were selected for operations, the first switch 302"(a) can be configured by the selection signal to connect the memory controller 31 to the first memory module 24 in a point-to-point data connection. This configuration of the two-way switches 302" substantially eliminates bus reflections from the unused portion of the bus 28. In the above example, the unused portion of the bus 28 includes the data paths between the first and second two-way switches 302"(a) and 302"(b) and the data paths connected to the second memory module 26.

FIG. 13 shows another exemplary embodiment of a bus and switch topology in accordance with the invention. The FIG. 13 structure is similar to that of FIG. 2. In FIG. 13, the two-way switches 302' are not located separately from the memory modules 24, 26, but instead are each located on a memory module 24, 26, like the FET switches shown in FIGS. 2 and 3. In this embodiment, each memory module 24 includes an interface circuit 30 that may have a two-way switch 302', connected to pass data between a first bus segment 28a and memory devices 54, 56, 58, 60, or between first and second bus segments 28a, 28b, depending on the state of the two-way switch 302'. Data may be passed between the memory controller 31 and a conversion circuit 45 on the first bus segment when the two-way switch 302' is in a first state, and when the two-way switch 302' is in a second state data may be passed between the first and second bus segments 28a and 28b. This topology permits point-to-point data communications between a memory module 24, 26 and the memory controller 31, when a given module 24, 26 is selected. In addition, the interface circuit 30 may also include a conversion circuit 45 as shown including a voltage converter 48, a multiplexer/demultiplexer 46 and a coder/decoder 47 for performing data rate, encoding, and voltage level conversions, as noted in connection with FIG. 2.

FIG. 14 shows another exemplary embodiment of a bus topology in which the two-way switches 302''' are located on the memory devices 54, 56, 60. For example, each of the memory devices 54, 56, 60 may be included on individual integrated circuit chips, and a two-way switch 302''' may also be located on the integrated circuit chip for each memory device 54, 56, 60. Each memory device 54, 56, 60 may be required to have an input and an output data path to connect the two way switches 302''' in the serial fashion illustrated in FIG. 14. In operation, the switches 302''' may be configured to select one of the memory devices 54, 56, 60 at a time for communications with the memory controller 31.

FIG. 15 illustrates another exemplary embodiment of the invention which combines the bus and switch topologies shown in FIG. 12 and FIG. 14. In this embodiment, a memory module 24, 26 is selected by the switches 302'', while a memory device is selected by the switches 302'''.

In FIGS. 12-15, although each of the segments of data bus 28 is shown for simplicity as a single line connected to a single switch, it is to be understood that each of the segments of the data bus 28 may include a plurality of data paths and would thus be connected to a respective plurality of two-way switches 302'. In addition, each of the two-way switches 302' may be included in an integrated interface circuit 30 of the type described above in connection with FIGS. 2 and 3, e.g., one example of which is shown in FIG. 13.

Referring back to FIG. 1, the integrated interface circuit 30 allows devices of different technologies to communicate and exchange data. For example, data may be exchanged between a processor and memory modules 24, 26 (either directly or through the memory controller 31) at high speed using the segmented data bus 28, while the second data bus 32 may connect to memory devices that operate at a lower speed. In this example, the slower data rate of the

bus 32 connected to the memory devices allows for the use of inexpensive memory integrated circuits (ICs).

Moreover, use of a segmented data bus 28 may permit the construction of a non-parallel terminated network of devices. Referring to FIG. 1, each of the devices on the bus, including the memory controller 31 and other system devices 24, 26, is connected to respective segments 28a, 28b, 28c of the segmented data bus 28 to form a "daisy chain." Such a bus system may permit implementation of a memory subsystem with smaller drivers of lower capacitance, lower voltage level in the individual segments 28a, 28b (i.e., reduced DC load current), and having decreased power consumption.

When a device is removed from segmented data bus 28, e.g., a memory module is absent, a low cost jumper 55 or other simple continuity module (CM) may be used to maintain the continuity of the bus 28, as shown in FIG. 8.

In addition, as shown in FIG. 18 programmable active termination may be used in combination with the switching circuits 39 in order to further improve data transfer performance. During data transmission between the memory controller 31 and a memory module 24, 26, programmable active termination at either the memory module 24, 26 or the memory controller 31 may be used to properly terminate the circuit elements during READ and WRITE operations. For example, referring to FIG. 18, a programmable terminator 452 may be located at the memory controller 31 and activated during READ operations to properly terminate the transmission path of the data at the memory controller 31. Another programmable terminator 452 may be located at each memory module 24, 26 and activated during WRITE operations to properly terminate the transmission path at the memory module 24, 26 that is the source of the READ data. The programmable terminators 452 may be programmed by the memory controller 31 or another mechanism for coordinating READ and WRITE

operations using, for example, a strap or hardwired data connection. For example, the programmable terminator 452 may be programmed using a pin or a register on the memory module 24, 26 or memory controller 31. Programmable active termination is further described in an application for patent with serial no. 09/659,334, entitled "ACTIVE TERMINATION IN A MULTIDROP MEMORY SYSTEM," filed September 12, 2000, and is incorporated by reference herein.

In addition, another exemplary embodiment of the invention may include switching circuits, e.g., FET switches 39, having programmable drive strength, for example as illustrated in FIG. 16. Each of the FET switches 39 may have a programmable drive strength controlled by the memory controller 31. For example, in FIG. 16 the drive strength of each of the p-channel FET switches 39 may be controlled by the voltage applied to the gate of the switch 39 as determined by the memory controller 31. One embodiment of the invention may use a different drive strength for one or more switches 39 depending on which memory module 24, 26 is selected for READ or WRITE operations.

FIG. 10 illustrates another exemplary processor system which may include a segmented data bus 28. Referring to FIG. 10, the processor system, which may be a computer system 100, for example, generally comprises a central processing unit (CPU) 102, for example, a microprocessor, that communicates with one or more input/output (I/O) devices 112, 114, 116 over a system bus 122. The computer system 100 also includes random access memory (RAM) 118, a read only memory (ROM) 120 and, in the case of a computer system may include peripheral devices such as a floppy disk drive 104, a hard drive 106, a display 108 and a compact disk (CD) ROM drive 110 which also communicate with the processor 102 over the bus 122. The RAM 118 includes memory devices communicating with a memory controller 31 via a segmented data bus 28 and

switches constructed in accordance with the invention. This configuration of the computer system 100 permits high speed communication and/or data transfer between different types of data devices, for example between the processor 102 and the memory controller 31 at the RAM 118. It should be noted that FIG. 10 is merely representative of many different types of processor system architectures which may employ the invention.

As noted, the segmented data bus 28 may be terminated by bus terminators, e.g., bus terminating resistors 38, located at the memory controller 31 as shown in FIG. 1, at one end of the bus 28 as shown in FIG. 8, at the interface circuit 30 as shown in FIGS. 2, 3 and 13, at the memory modules 24, 26 as shown in FIG. 12, and/or at each memory device 54, 56, 60 as shown in FIG. 14. The bus terminating resistors 38 may be switched terminators to permit switchable termination (i.e., termination enabled (ON) or termination disabled (OFF)) for varying data transfer operations. An exemplary switched terminator 38 may also provide source termination for alleviation of the effect of bus reflections, improving data transfer performance.

Although the segmented data bus 28 has been described with reference to a digital data system, e.g., a memory system having memory modules 24, 26, the segmented data bus 28 can be used to transmit signals of any types, including analog, digital and radio frequency (RF) signals.

While the invention has been described and illustrated with reference to specific exemplary embodiments, it should be understood that many modifications and substitutions can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as limited by the foregoing description but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is: